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Name of Examination : **Winter 2020** - (Preview)

Course Code & Course Name : **CO202U - Digital Electronics and Logic Design**

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Maximum Marks : **60**

Duration : **3 Hrs**

[Edit](#) [Print](#) [View Answer Key](#) [Close](#) **Answer Key Submission Type:** Marking scheme with model answers and solutions of numerical

Instructions:

1. All questions are compulsory.
2. Illustrate your answer with suitable figures/sketches wherever necessary.
3. Assume suitable additional data; if required.
4. Use of logarithmic table, drawing instruments and non programmable calculators is allowed.
5. Figures to the right indicate full marks.

1) Solve any three sub-questions.

- a) State and verify De-Morgan's theorem. [6]
- b) Minimize the expression using k-map. [6]

$$Y = \sum m(1, 3, 7, 11, 15) + d(0, 2, 5)$$
- c) State the types of shift registers. Explain any one and give the applications. [6]
- d) Draw neat circuit diagram of clocked Jk- flip flop using NAND gates. Explain race around condition. [6]

2) Solve any three sub-questions.

- a) Design a binary to gray code converter and draw circuit diagram. [6]
- b) i. Convert $(111101100)_2$ to octal equivalent. [1]
 ii. Convert $(634)_8$ to binary. [1]
 iii. Convert $(725.63)_8$ to binary [1]
 iv. Convert $(3FD)_H$ to binary. [1]
 v. Convert $(615)_8$ to hexadecimal. [1]
 vi. Convert $(567)_8$ to decimal. [1]
- c) Implement Boolean expression for Ex-NOR gate using NOR gate. [6]
- d) Design 1:8 demultiplexer using two 4:1 demultiplexers. [6]

3) Solve any three sub-questions.

- a) Give comparison between combinational circuits and sequential circuits. [6]
- b) Implement full adder using half adder circuit. [6]
- c) What are the different types of read only memory(ROM). Explain. [6]
- d) Give comparison between synchronous and asynchronous counters. [6]

4) Solve the following sub-questions.

- a) Compare static and dynamic random access memory. [3]
- b) Implement half subtractor using basic gates [3]

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